Topic: **Technology Mapping and Dynamic Programming**

Technology mapping is the phase of logic synthesis when gates are selected from a technology library to implement the circuit. Technology mapping is normally done after technology independent optimization.

**Exercise 1**

In this exercise, a Boolean function and a library cell are given. You are required to do the following steps:
- Decomposition
- Pattern matching
- Covering

In Figure 1 the cells of the library and their cost are given. The cost could be area, time or power. The objective is to minimize the cost.
### Table

<table>
<thead>
<tr>
<th>Cells</th>
<th>Cost</th>
<th>Symbol</th>
<th>Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVERTER</td>
<td>2</td>
<td><img src="image" alt="Symbol" /></td>
<td><img src="image" alt="Pattern" /></td>
</tr>
<tr>
<td>NOR2</td>
<td>3</td>
<td><img src="image" alt="Symbol" /></td>
<td><img src="image" alt="Pattern" /></td>
</tr>
<tr>
<td>NOR3</td>
<td>4</td>
<td><img src="image" alt="Symbol" /></td>
<td><img src="image" alt="Pattern" /></td>
</tr>
<tr>
<td>NOR4</td>
<td>5</td>
<td><img src="image" alt="Symbol" /></td>
<td><img src="image" alt="Pattern" /></td>
</tr>
<tr>
<td>AOI21</td>
<td>4</td>
<td><img src="image" alt="Symbol" /></td>
<td><img src="image" alt="Pattern" /></td>
</tr>
</tbody>
</table>

**Figure 1**

**Questions:**

1.1 **1.1 Decompose the following function using the base functions:** NOT, NOR2.
Show each decomposition you make. For example:

1.2 Match the all of the patterns in figure 1 to the decomposed circuit. How many cells of each type have you found?
1.3 Add inverter pairs to each junction of the decomposed circuit and repeat Q2.
1.4 What is the trivial covering solution cost (Q2)? (The trivial covering solution consists of only inverters and nand2 cells)
1.5 Find 1 or 2 other better covering solutions, by using the decomposed circuit of Q3.
1.6 Consider the following circuit. The cost of the cells is Nor2: 2 and Inverter: 1. You are allowed to use only Nor2 and Inverter cells, what is the cost of the circuit?

1.7 Now you can use the cell AOI21 from Figure 1 (see above) that has the cost of 4. Does your cost improve?

1.8 Can simulated annealing be applied to the technology-mapping problem? If so, describe how you will do it. If not, explain briefly why it isn’t feasible.
**Exercise 2**

Consider logic network made of inverters and 2-input NANDs. We have labeled the internal nodes of the network with numbers 1-12 for convenience.

Suppose your technology library consists of:
1 input gates: INVERTER (cost 1)
2 input gates: NAND (cost 2), AND (cost 3), NOR (cost 2)
3 input gates: NAND (cost 3), OAI21 (cost 3) (or-and-invert, it implements \((a+b)\cdot c\)

Do this:
- First, draw the target patterns for each of these library cells, as they consist of NAND2s and INVERTERs.
- For each node of the network, write which library patterns match at this node.
- Run dynamic programming algorithm presented in class on this network and find minimum cost cover. Show how the best cover is determined by backtracking on the tree.
Exercise 3 – Delay-optimal technology mapping based on dynamic programming (optional)

Consider optimal tree covering algorithm presented in the class. We would like now to extend the algorithm to be able to find minimal tree cover so that the tree satisfies delay constraints. Let’s assume that each pattern in the library has delay cost $D_i$ in addition to area cost $A_i$, and the delay cost of pattern doesn’t depend on load capacitance on pattern’s root. Pattern’s delay cost is the maximal delay of each one of the pattern’s input pins to its root. It is required to design an algorithm that will find minimal cover of tree such that the maximal delay from one of tree leaves to the root will be less than given value $T$.

Answer the following questions:

3.1 What is the number of stages (overlapping sub-problems) that should be solved in the new problem? Does it differ from basic problem case?

3.2 In the algorithm shown in the class, the state (solution of sub-problem) was characterized by the area cost of underlying sub-tree. How the state will be characterized in the new algorithm?

3.3 How state expansion is performed in the new algorithm? If the number of states before expansion is $m$ and the size of pattern library is $P$, what is the number of states after expansion?

3.4 How state pruning is performed in the new algorithm? What is the order of growth of number of states from stage to stage? Hint: understand when the generated state is redundant. For example, one of two states is redundant if both states have the same area cost, but ...

3.5 What is the number of states in the root?

3.6 Assume that each solution obtained in the root is placed on the Area-Delay plane. If all points representing different solutions are connected by the curve, how this curve will look like? What fundamental property of solutions in the root can be derived from this?

3.7 Explain how solutions satisfying given delay requirements are selected and how the best solution is chosen.

3.8 What is the run-time and space complexity of the modified algorithm?