CAD for VLSI

Tutorial #14

Delay Modeling

Figure 35: Delay for Local and Global Wiring versus Feature Size
Previous Assumptions

• Many simplifying assumptions have been made
  – Fixed gate delays.
  – Equal rise/fall times.
  – Ideal input waveforms.
  – No delay along wires.

• Wires cause delays. In DSM wire delay is very significant and cannot be ignored.
ITRS Predictions

The International Technology Roadmap for Semiconductors.

Bottom line: Scaling decreases gate delays and increases long wires delays!
Wire Delay Modeling

- Wires have a resistance and a capacitance
- If we assume that the resistance and capacitance of a single wire can be **lumped**:

\[
V_{\text{out}}(t) = (1 - e^{-t/RC})
\]

For a unit step function at \( V_{\text{in}} \):

\[
V_{\text{out}}(t) = (1 - e^{-t/RC})
\]
Wire Delay - Distributed

- In actual fact the resistance and capacitance are distributed along the wire:

```
Vin  R  Vout
    /   |
   /    C
```

- No simple closed form expression exists for $V_{out}$.
- Non trivial mathematics enable us to compute $V_{out}$ for a distributed line.
- Note, as the capacitance is distributed all along the line, the current changing the capacitance at the beginning of the line, does not “see” all of the resistors at once.
Lumped Circuit Approximation for a Distributed Line

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \text{Vout} \]

\[ \text{L model} \]

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \text{C} \quad \frac{C}{2} \]

\[ \Pi\text{-model} \]

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \text{Vout} \]

\[ \text{T-model} \]

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{3} \quad \frac{R}{3} \quad \frac{R}{3} \quad \text{Vout} \]

\[ \Pi\text{-model} \]

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{3} \quad \frac{R}{3} \quad \frac{R}{3} \quad \text{Vout} \]

\[ \Pi\text{-model} \]

\[ \text{Vin} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{2} \quad \frac{R}{3} \quad \frac{R}{3} \quad \frac{R}{3} \quad \text{Vout} \]

\[ \Pi\text{-model} \]

\[ \Pi3\text{-model gives error of less than 3\% compared to the distributed model} \]

Schematic RC Trees

- Based on estimation of the P&R.
- Every net segment is replaced by an equivalent distributed RC model.
- For example - the 4 segments are replaced by Π models.
Layout RC Trees

- Based on extraction from the layout.
- Every polygon is replaced by an equivalent distributed RC model.
- The same example.

Simplified Layout

Simplified Layout - polygons
Layout RC Trees

- More complex RC net. Nets can have thousands of polygons.
- Ignoring - Vias, coupling.
- Is it useful to simplify the net?
RC Delay Estimation

- Computing $V_{out}$ using accurate circuit analysis is very time consuming for large nets.
- Mostly an approximate, easy to compute heuristic is used.
The Elmore Delay

- In the 1940s, Elmore derived a formula to compute delay.
- The method was applied by Penfield, Rubenstein and Horowitz in 1980s for RC trees.
- Easy to compute.
- Can be easily incorporated into automatic layout generation algorithms.

Naming Conventions

- Resistor $R_i$ feeds into node $i$
- Capacitor $C_i$ is connected between node $i$ and gnd
The Elmore Delay

- \( V_{\text{out}} = V_3 \) is approximated as: \( V_3(t) = V_0(1 - e^{-t/\tau}) \)
- Using a single time constant \( \tau \), computed by Elmore’s formula.
- Every output (and internal node) has a different constant \( \tau \).
The Elmore Delay Formula

\[
\tau_k = \sum_{i=0}^{i=k} R_i \left( \sum \text{all downstream caps in complete network from node i} \right)
\]

• \(R_i\) are the resistances on path from node 0 to node k.
  – i.e \(R_i = R_0, R_1, \ldots, R_k\)
  – Note, the above includes only resistors in the path from 0 to k, thus the index 0 to k may not necessarily include all integers between 0 and k.

• \(C_i\) is the capacitance at node I.

• \(R_i\) is multiplied by all capacitors which are charged/discharged by the current passing through \(R_i\).
Exercise 1

• For the circuit given in the following schematic:
  – replace the driving gate by a voltage source and a resistor
  – replace the driven gates with a load capacitor
  – represent all wire segments with their corresponding Π-models
  – compute the resistances and capacitances of each Π-model
    given that: \( R = r \cdot L/W \) (\( r = 1/2 \)) ; \( C = c_a \cdot L \cdot W \) (\( c_a = 2 \))

• Calculate a value of “w” for which the delay at each of the leaves is equal.
Exercise 1 - RC Net

\[ R = r_r \times \frac{L}{W} \quad (r_r = 1/2) \quad ; \quad C = c_a \times L \times W \quad (c_a = 2) \]
Exercise 1 - RC Net

\[ R = r_\ast \frac{L}{W} \ (r_\ast = 1/2) ; \quad C = c_a \ast L \ast W \ (c_a = 2) \]
Exercise 1 - RC Net - simplified

\[ R = r_\ast \frac{L}{W} \quad (r_\ast = 1/2) \; ; \; C = c_a \ast L \ast W \quad (c_a = 2) \]
Exercise 1 - Compute downstream cap.

- Downstream capacitances
  - 0:
  - 1: \( R = \frac{r}{2} \frac{L}{W} \) (\( r = 1/2 \)); \( C = c_a L W \) (\( c_a = 2 \))
  - 2:
  - 3:
  - 4:
  - 5:
  - 6:
Exercise 1- Compute downstream cap.

- Downstream capacitances
  - 0: $8 + (16+w) + 9 + (12+w) + 5 + 5 + 5 = 60 + 2w$
  - 1: $52 + 2w$  \((60 + 2w - 8)\)
  - 2: 9
  - 3: $(12+w) + 5 + 5 + 5 = 27 + w$
  - 4: 5
  - 5: 5
  - 6: 5
Exercise 1 - Solution

\[ \tau_k = \sum_{i=0}^{i=k} R_i \] (\( R_i \) are the resistances on path from node 0 to node k)

\( R_i \) are the resistances on path from node i to complete network from node i

\[ \tau_{04} = \tau_{05} = \tau_{06} = 3 \times (60+2w) + 4 \times (52+2w) + 1/(2w) \times (27+w) + 2 \times 5 \]
\[ = 180 + 6w + 208 + 8w + 13.5w + 0.5 + 10 \]
\[ = 398.5 + 14w + 13.5/w \]

\[ \tau_{02} = 3 \times (60+2w) + 4 \times (52+2w) + 4 \times 9 \]
\[ = 180 + 6w + 208 + 8w + 36 \]
\[ = 424 + 14w \]

For the delays to be equal:
\[ 398.5 + 14w + 13.5/w = 424 + 14w \]
\[ \Leftrightarrow 13.5/w = 25.5 \implies w = 13.5 / 25.5 = 0.529 \]

• Downstream capacitances:
  • 0 : 60+2w
  • 1 : 52+2w
  • 2 : 9
  • 3 : 27+w
  • 4 : 5
  • 5 : 5
  • 6 : 5

• Downstream resistance: \( r_0=3, r_1=4, r_2=4, r_3=1/(2w), r_{456}=2 \)
• What exactly is the gate / wire delay?

**Gate only:**
\[ t_d = R_{\text{eff}} C_L \]

**Gate with lumped wire:**
\[ t_d = (R_{\text{eff}} + R_i) C_L = R_{\text{eff}} C_L + R_i C_L \]

**Gate with \( \Pi \) modeled wire:**
\[ t_d = R_{\text{eff}} (C_i + C_L) + R_i (C_i/2 + C_L) \]

It is difficult to separate between the gate delay and the wire delay.

This subject is widely covered by:
Complete Network Delay

• What the delay of the following network?

• An inaccurate result will be obtained if the delay of the above network is computed by computing separately the gate delays and the wire delays.

• A more accurate result for the delay can be obtained if the basic delay unit for which we compute the delay is composed of both the inverter and interconnect wire connected to its output.
Elmore Delay - Limitations

Resistors Shielding

- \( \tau_{02} = 424 + 14w \) i.e. the same as before.
- However:
  We know that the huge resistors will act as disconnections and the capacitors downstream will be shielded.
- For a more accurate result - the capacitors at nets 4, 5, 6 should be ignored.
The Elmore delay works for a single driver net, as most nets are.

However:
Most nets are also cross coupled to their neighbors!

The cross capacitance has major effect on the delay and the correctness of the Elmore delay.
Elmore Delay - Limitations

Cross Coupling - Decoupling

- Using Miller’s theorem (taught in the linear circuits course).
- The cross-capacitor is replaced by equivalent two capacitors, whose size is Miller’s factor times the original capacitance.
- Miller’s factor can be assumed to be in the range of \([0..2]\) depending on the switching on both sides of the cross capacitor.
  - Actually can be in range \([-1; 3]\)
- This allows delay estimation with Elmore’s delay.
Comments

- A complete derivation of Elmore’s formula can be found at: [http://www.ece.cmu.edu/~ee760/760docs/lec18.pdf](http://www.ece.cmu.edu/~ee760/760docs/lec18.pdf)

- DFS can be used to efficiently compute the node capacitances - the recursion folding returns the downstream capacitors to the resistor nodes.