Logic CAD of VLSI (046880)

http://www.ee.technion.ac.il/courses/046880/index.html

Spring Semester – 2017

Administration information

Classes:

**Lecture:** Wednesday 8:30-10:30 Meyer 351

**Recitation:** Wednesday 10:30-11:30 Meyer 351

Staff:

**Instructor:**
Dr. Eitan Zahavi
Office: TCE, Phone: 074-723-7208 but much better in email below.
Reception hours:
    With email coordination Wed 11:30 @ TCE
Email: zahavi.eitan@gmail.com

**Teaching Assistant and Homework checker:**
Mr. Ziv Berkovich
Office: Meyer 1134, Phone: 3298
Reception hours:
    With email coordination Wed 11:30 @ Meyer 1134
Email: zivber@tx.technion.ac.il

Grading:

Grades will be based on:

- **Homework** 50% compulsory
- **Final exam.** 50% compulsory
**Homework Policy:**

- Homework assignments will be given almost every week, but you don’t need to hand-in all of them. There is a choice of homework options, see next.
- Homework should be submitted **in pairs** and **electronically-only** using the moodle system according to submission dates being published in the website.
- If you experience difficulties making the necessary drawings electronically – do your assignment using pencil & paper and submit a scanned version. Electronic submission does not mean an excuse from detailed equations and unclear schematic drawings.
- In order to get full grade on Homework  (Wet 40% Dry 10%) you must hand-in:
  3 (out of 5) programming exercises (Wet).
  3 (out of 5) regular “pencil & paper” exercises (Dry).
- Late submission: is allowed (automatically) in case of reserve duty accompanied by a prior notification by e-mail and the reserve slip attached to the submitted work.

**Final exam:**

Dates, Times, and Places:

1. 28.07.2017  Fri  00:00-00:00  Room: XXX 000
2. 16.10.2017  Mon 00:00-00:00  Room: XXX 000